**Continuous Assessment Test – II**

**Programme Name & Branch: B.Tech CSE**

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| **Course Name & Code: CSE1003 & Digital Logic and Design** | | |
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| **Exam Duration: 90 Minutes Slot: C1+TC1** | | **Maximum Marks : 50** |

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| **Answer All Questions PART A 4 x 5 = 20 Marks** | | |
| **Q.No** | **Question** | **Marks** |
|  | Consider the following combinational circuit, | 5 (CO3) |
|  | Design an octal to binary encoder with its logic circuit, truth table and its output Boolean function. | 5 (CO4) |
|  | Convert SR flip-flop into JK flip-flop using truth table and excitation table. Draw the converted JK flip-flop with necessary inputs. | 5 (CO5) |
|  | Calculate and Compare the Total Propagation Time of 4-bit Ripple Carry Binary Parallel Adder (BPA) and 4-bit BPA with Look-Ahead Carry Generator for the following timing specifications:  a. XOR - 40ns  b. AND – 25ns  c. OR – 15ns | 5 (CO4) |
| **Answer All Questions PART – B 3 x 10 = 30 Marks** | | |
| **Q.No** | **Question** | **Marks** |
|  | An ABCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder *(a, b, c, d, e, f, g)* select the corresponding segments in the display, as shown in Figure (a) . The numeric display chosen to represent the decimal digit is shown in Figure (b) . Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates. The six invalid combinations in BCD should result in a blank display.    Figure (a) Figure (b) | 10 (CO3) |
|  | Implement the following Boolean function using multiplexer | 10 (CO4) |
|  | Design a full adder using 3 to 8 line decoder. The decoder uses only the basic AND and NOT gates.   * 1. Draw the logic circuit of full adder      * 1. Give the truth table for full adder output Sum and Carry      * 1. Derive the Boolean expression for D0 through D7, Sum and carry | 10 9CO4) |